

IN THE SPECIFICATION

Please amend the paragraphs of the specification as follows:

Please amend paragraphs [0014], [0015] [0029], [0031], [0057], [0064], [0077], [0080] and [0082] as follows:

[0014] The need in the art is addressed by the system for reducing current leakage in an integrated circuit of the present invention. In the illustrative embodiment, the inventive system is adapted for use with ~~Complimentary~~ Complementary Metal Oxide Semiconductor (CMOS) latches. The system includes a first circuit component and a second circuit component in a path between a relative high voltage and a relatively low voltage. A mechanism selectively provides feedback from an output of the second circuit component to an input of the first circuit component to selectively cutoff the path at the first circuit when the path is not cutoff at the second circuit.

[0015] In a more specific embodiment, the mechanism further includes a mechanism for preserving data in the integrated circuit. The mechanism for preserving data in the integrated circuit includes a multiplexer for selectively enabling the feedback when the integrated circuit is in sleep mode. The multiplexer is a 2-1 multiplexer having a shift input as a control input and having scan-in and feedback inputs.

[0029] The master cell 12 includes a first column of transistors 34 and a second column of transistors 36 that act as selectively gated inverters, as discussed more fully below. The first column of transistors 34 includes, from top to bottom, a first High Voltage Threshold (HVT) NMOS (N-channel Metal Oxide Semiconductor) transistor T1, a second Low Voltage Threshold (LVT) NMOS transistor T2, a third LVT PMOS (P-channel Metal Oxide Semiconductor) transistor T3, and a fourth HVT PMOS transistor T4. The transistors T1-T4 are connected so that the source of the fourth PMOS transistor T4 is connected to a high voltage state (Vdd), which is typically provided via a DC voltage source (not shown). The drain of the PMOS transistor T4 is connected to the source of the third PMOS transistor T3. The drain of the third PMOS transistor T3 is connected to the drain of the second NMOS transistor T2. The source of the second NMOS transistor T2 is connected to the drain of the first NMOS transistor T1. The source of the first transistor NMOS transistor T1 is connected to a low voltage state, such as

ground. Hence, the first column of transistors 34 are connected so that if the transistors T1-T4 were all on, current would flow from the high voltage state to the low voltage state from the source of the fourth PMOS transistor T4 through to the source of the first NMOS transistor T1.

[0031] The shift input 20 and the sleep input 22 of the master cell 12 are input to an OR gate 38. The output of the OR gate 38 is connected to the input of a first HVT inverter I1; to the gate of the fourth HVT PMOS transistor T4 in the first column of transistors 34; and to the gate of the eighth NMOS transistor T8 in the second column of transistors 36. The output of the first inverter I1 is connected to the gate of the first HVT NMOS transistor T1 and to the gate of the fifth HVT PMOS transistor T4.

[0057] The system 80 includes a 2-1 multiplexer (MUX) 82, a controller 84, additional circuitry 88, a first low-leakage inverter 92, intervening circuitry ~~[[84]]~~ 94, a second low-leakage inverter 96, additional intervening circuitry 98, and a third low-leakage inverter 100. The MUX 82 receives a control input (SHIFT) 20 from a controller 84. A first MUX input 86 originates from the additional circuitry 88. The additional circuitry 88 may provide an output (SIN) 86 to be scanned into a latch (see Fig. 1). Alternatively, the first MUX input 86 may originate from the controller 84. A second MUX input (IQ) 90 originates from an output of the third low-leakage inverter 100. The input of the third low-leakage inverter 100 originates from the additional circuitry 88, which may represent the last stage of a slave latch (see 14 of Fig. 1). The output of the third low-leakage inverter 100 is also connected to the additional intervening circuitry 98. The additional intervening circuitry 98 is also connected to an output of the second low-leakage inverter 96. An input of the second low-leakage inverter 96 is connected to the intervening circuitry 94, which is also connected to an output of the first low-leakage inverter 92. An input of the first low-leakage inverter is connected to an output of the MUX 82.

[0064] Fig. 4 is a diagram of a high-performance, low-leakage latch 110 constructed in accordance with the teachings of the present invention, which can operate effectively when the clock sleeps high or low, and which incorporates the system 80 for reducing leakage of Fig. 3. The high-performance characteristics of the latch ~~[[10]]~~ 110 enable the use of a more efficient clock signal 24', inverted clock signal 26', master slave output signal 28', and data signal 18'. The clock signal 24' may have a higher frequency and a narrower pulse width. The data signal

18' may ~~[[have]]~~ also have a narrower pulse width, which affects the master slave output 28' and the output signal 30', as discussed more fully below.

[0077] Those skilled in the art will appreciate that various modifications to the latch 110 may be made to meet the needs of a given application without departing from the scope of the present invention. For example, the fifth HVT inverter I5 and the eight HVT inverter I8 may be replaced with LVT inverters. In this case, an additional last stage transistor (not shown), such as the transistor T20 used for the slave LVT inverters I6, I7, would be included with the inverters I5, I8 to ensure that leakage is minimized during sleep mode. Furthermore, ~~[[thee]]~~ the scan-in and scan-out functionality of the latch 110 may be omitted without departing from the scope of the present invention.

[0080] Fig. 6 is a diagram of a first alternative embodiment 130 of the latch 110 of Fig. 4 lacking the MUX 82 but employing an integrated MUX implemented, in part, via a set of additional HVT transistors 132. The MUX implemented via the transistors 132 is integrated with the master cell 12". The second column of transistors 36 is fitted with the additional HVT transistors 132, which include, from top to bottom, a fortieth PMOS transistor T40, a forty-first PMOS transistor T41, a forty-second PMOS transistor T42, a forty-third NMOS transistor T43, a forty-fourth NMOS transistor T44, and a forty-fifth NMOS transistor T45. The source of the fortieth transistor T40 is connected to a high voltage state represented by Vdd, while the drain is connected to the source of the fifth transistor T5 and the source of the transistor T41. The PMOS transistor T40-T42 are connected drain-to-source, and the NMOS transistors T43-45 are connected drain-to-source. However, the drain of the forty-second PMOS transistor T42 is connected to the drain of the forty-third NMOS transistor T43. The drain of the forty-fifth NMOS transistor T45 is connected to the source of the transistors T44 and T8.

[0082] The operation of the latch 130 is similar to the operation of the latch 110 of Fig. 4 with the exception that the functionality of the MUX 82 of the latch 110 of Fig. 4 is implemented via the columns of transistors 36 ~~and 132~~ and the MUX inverter 124 of the latch 130 of Fig. 6. When the latch 130 is in sleep mode, the half-latch feedback 90 ensures that the leakage paths ~~though~~ through the inverters (I4) 96 and (I9) 100 are cutoff. Hence, the pass gates 42 and 114 may be implemented as high-speed LVT pass gates without comprising leakage characteristics.

Please delete paragraph [0088] as follows:

**[0088]** ~~Accordingly,~~